STRAINED DISLOCATION-FREE CHANNELS FOR CMOS AND METHOD OF MANUFACTURE

ABSTRACT

A semiconductor device and method of manufacturing a semiconductor device. The semiconductor device includes channels for a pFET and an nFET. An SiGe layer is grown in the channel of the nFET channel and a Si:C layer is grown in the pFET channel. The SiGe and Si:C layer match a lattice network of the underlying Si layer to create a stress component in an overlying grown epitaxial layer. In one implementation, this causes a compressive component in the pFET channel and a tensile component in the nFET channel. In a further implementation, the SiGe layer is grown in both the nFET and pFET channels. In this implementation, the stress level in the pFET channel should be greater than approximately 3 GPa.

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